UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,029,963 B2
APPLICATION NO. : 09/943078
DATED : April 18, 2006
INVENTOR(S) : Todd R. Abbott

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 4, line 27 "the is isolation" should read --the isolation--;

Col. 7, line 38 "resistano" should read --resistance--; and

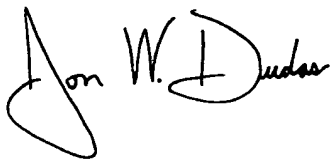
Col. 12, Claim 4 should be added as follows:

4. The method of fabricating a semiconductor device of claim 1, further comprising:

shaping said spacer layer to form spacers against the vertical walls of said damascene gate structure and said damascene interconnect structure.

Signed and Sealed this

Third Day of October, 2006



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Director of the United States Patent and Trademark Office